IN THE CLAIMS

Please amend the claims as follows:

Sub. B1

1. (amended) In an [An] inverter for producing an AC output voltage from a source of DC voltage connected therewith and[circuit connected to a load and] having a pair of alternately conducting switching transistors, each having a base [base-emitter junction,] and [adapted to convert] being connected with said DC voltage [supplied from a DC] source [having positive and negative terminals into an AC output voltage], an improved drive circuit for said transistors, comprising:

first [drive circuit]means connected [between] with the [base-emitter junctions] bases of the transistors for alternately providing drive signals thereto, said first means being responsive to conduction of the conducting one of said transistors for applying a [and operable to provide intermittent] positive feedback signal thereto [signals for causing the alternating conduction of the transistors]; [and]

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second [drive circuit] means [also] connected with [between] the bases [base-emitted junctions] of the transistors for alternately providing drive signals thereto, said second means being responsive to conduction of the conducting one of said transistors for applying a negative [and operable to provide intermittent subtractive] feedback [signals for rapidly turning off a conducting transistor whereby an alternating current is caused to flow through the load.] signal thereto having a magnitude less than that of the positive feedback signal; and

control means associated with the first means for terminating said positive feedback signal prior to termination of said negative feedback signal whereby the drive being applied to said conducting transistor rapidly reverses in polarity.

2. (amended) The inverter circuit of Claim 1 wherein[:] said first [drive circuit] means includes a [saturable] current transformer for providing said positive feedback signals with a magnetic core.

3. (amended) The inverter circuit of Claim 2 wherein[:] said control means includes a saturable magnetic core for said transformer, [current transformer is effective to deliver a] said core causing termination of said positive feedback signal [until such time as said core] when it becomes saturated.

4. (amended) The inverter [circuit] of Claim[1] 3 wherein[:] said second [drive circuit] means includes a second [non-saturable] [current] transformer connected with said transistors for providing said negative feedback signals.

5. (amended) The inverter [circuit] of Claim 4 wherein[:] said [non-saturable] second transformer has a non-saturable core and continues to provide [delivers] said [subtractive] negative feedback signals after [said] the core of said first [drive circuit means] transformer becomes saturated.

6. (amended) The inverter [circuit] of Claim 5 wherein[:]

said first [current] transformer has an output winding [is] connected [to] between the [base-emitter junction of each] bases of said pair of switching transistors, and

said second current transformer has an output winding [is also] connected [to a base-emitter junction] between the bases of [each of] said pair of switching transistors.

7. (amended) The inverter [circuit] of Claim 5 including:

a DC voltage source with positive and negative terminals;

a power output transformer having[a] an input winding with a center-tap connected to one of said terminals [the positive terminal] of the DC source; and

said second current transformer has [a] an output winding with a center-tap connected to the [negative] other terminal of the DC source.

Sub. B3

8. (amended) The inverter [circuit] of Claim 1 wherein[:] said drive circuit and said pair of switching transistor [is self-oscillating for controlling the conduction of the switching transistors] self-oscillate.

9. (amended) The inverter circuit of Claim 1 wherein[:] each of the switching transistors has a collector element[;], and including

a capacitor [is] connected between said collector elements to restrain the rate of rise of collector voltage after transistor turn-off.

10. (amended) The inverter circuit of Claim 1 including[:]

a power output transformer with some shunt leakage inductance, [also] said output transformer being connected [to] between the collectors of the transistors.

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11. (amended) An inverter circuit connected to a load and having a pair of switching transistors connected in series across a source of DC voltage, with each transistor having a base-emitter junction, and adapted to convert DC voltage supplied from the DC source into an AC output voltage, comprising:

first drive circuit means connected between the base-emitter junction of the transistors and operable to provide intermittent positive feedback [signal] signals for causing the alternating conduction of the transistors; and

second drive circuit means also connected between the base-emitter junction of the transistors and operable to provide intermittent [subtractive] negative feedback signals for rapidly turning off a conducting transistor after the positive feedback signal thereto has terminated whereby an alternating current is caused to flow through the load.

14. (amended) The inverter circuit of Claim 12 including:

a power output transformer connected between the transistors and said voltage divider and operable to deliver to the load an AC output voltage produced by the alternating conduction of the transistors [to the load].

sub B4 15. (amended) An electrical inverter circuit [having a pair of alternately conducting switching transistors, each with a collector and base-emitter junction and adapted to convert] for converting a unidirectional input voltage into an alternating output voltage, comprising:

a2 a pair of alternately conducting switching transistors each having a collector-emitter and base-emitter junctions; and

drive control means effective to provide [subtractive bias means] reverse bias to the base-emitter junctions of both transistors during periods when their collector-emitter voltages are significantly greater than the transistor collector-emitter saturation voltages.

21. (amended) The inverter circuit of Claim 15 wherein:

said reverse [subtractive] bias means includes a non-saturable current transformer.

22. (amended) An electrical inverter circuit, comprising: [containing]

a3 a pair of alternately conducting switching transistors, each having a collector, base and emitter, and adapted to convert a unidirectional input voltage into an alternating output voltage, [and with] each of said transistors [transistor] having a cyclical emitter-collector voltage waveform characterized by four distinct periods within each cycle, namely: a period when the magnitude is low and substantially constant, a period when it increases rapidly, a period when it is high and substantially constant, and a period when it decreases rapidly; and[including:]

drive control means connected to the base-emitter junction of each transistor and operable to maintain each reversely biased during all periods other than the period when its voltage is low and substantially constant.

24. Please cancel Claim 24 without prejudice.

25. (amended) An electrical inverter circuit containing a pair of alternately conducting switching transistors, each having a collector and base-emitter junction, and adapted to convert a unidirectional input voltage into a cyclical, trapezoidal shaped, alternating output voltage, comprising:

control means connected to said transistors and operable to effect alternating periodic conduction thereof, said control means supplying to the base-emitter junction of each transistor a control signal effective to turn on a transistor only after its collector voltage has dropped substantially to its lowest level prior to said control signal being supplied thereto.

31. (amended) The inverter circuit of Claim 25 wherein:

said control means functions to render the inverter circuit [is] self-oscillating.

33. (amended) The inverter circuit of Claim 32 wherein:

a first diode shunting the base-emitter junction of a first transistor is operable to function as a clamp [so as] to limit the voltage rise at the collector of said second [first] transistor to twice the magnitude of the unidirectional input voltage.

34. (amended) The inverter of Claim 33 including:

a shunting diode connected across the base [collector] emitter terminals of each transistor.

Sub. B7

35. (amended) A push-pull electrical inverter circuit having a pair of alternately conducting switching transistors, each having a control input element, and adapted to convert a unidirectional input voltage into an alternating output voltage comprising:

first drive control means including saturable current feedback means for supplying [positively conducting] control signals to the control input element of each transistor <u>having a polarity supporting the conduction of the transistor</u>; and

second drive control means including non-saturable current feedback means for supplying [subtractive] control signals to the control input element of each transistor after said first saturable feedback means has saturated <u>having a polarity opposite to that of the first drive control means</u> whereby a conducting transistor is rapidly and efficiently turned off.

36. (amended) An electrical inverter circuit having a pair of switching transistors, each with a control input element, and adapted to convert a unidirectional input voltage supplied from a source having a pair of input terminals into an alternating output voltage comprising:

a series connection of the two transistors between the input terminals;

first saturable feedback means connected to the control input elements of the transistors for supplying [positive] control signals <u>thereto to turn them on</u>; and

second non-saturable feedback means also connected to the control input elements of the transistors for supplying [subtractive] control signals for alternately turning off a transistor.

Please add new Claims 37-44,as follows:

Sub. B8

37. In an inverter for producing an alternating output signal from a source of DC voltage connectable therewith and having a pair of switching transistors, an improved drive circuit, comprising:

a first drive means for alternately providing a first drive signal to said pair of switching transistors, said first drive signal tending to cause the transistor to which it is provided to assume a conductive state;

a second drive means for alternately providing a second drive signal to said pair of switching transistors, said second drive signal tending to cause the transistor to which it is provided to assume a nonconductive state, said second drive signal being provided to said transistor ptomptly after termination of provision of said first drive signal thereto.

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38. The inverter of claim 37 in which

said first and second drive signals are alternately, simultaneously provided to said transistors but have relative magnitudes which causes the transistor to which both drive signals are provided simultaneously to assume a conductive state, and

said inverter includes means associated with the first drive means for terminating said first drive signal being applied to the conducting one of said transistors prior to termination of provision of said second drive signal thereto to allow said second drive signal to rapidly turn off the conducting transistor.

39. The inverter of claim 38 in which said first drive means is a saturable device.

40. The inverter of claim 39 in which said saturable device is a saturable inductor.

41. The inverter of claim 38 in which said first and second drive signals are provided to each transistor in response to conduction of that transistor.

42. The inverter of claim 37 in which

another signal is developed in response of said second drive signal which could cause said transistors to turn on at an inappropriate time if applied thereto, and

said drive circuit includes means for preventing said other signal from being applied to said transistors.

43. The inverter of claim 42 in which said preventing means includes a diode.

44. The inverter of claim 38 in which said first drive signal is applied to one of said transistors only after the second drive signal has been applied to the other transducers for a sufficient time to insure that it is completely off.

REMARKS

In the foregoing amendment, applicant has amended the specification to correct the minor errors kindly noted by the Examiner.

In addition, Claims 1-11, 14-15, 21-22, 24-25, 31 and 33-36 have been amended to more clearly define applicant's invention and to overcome the various rejections to the claims under 35 USC § 112. It is believed that all of the claims do now meet with the requirements of the second paragraph 35 USC § 112, and withdrawal of the objection to the claims on that basis is therefore respectfully requested.